

FIG. 1 (PRIOR ART)

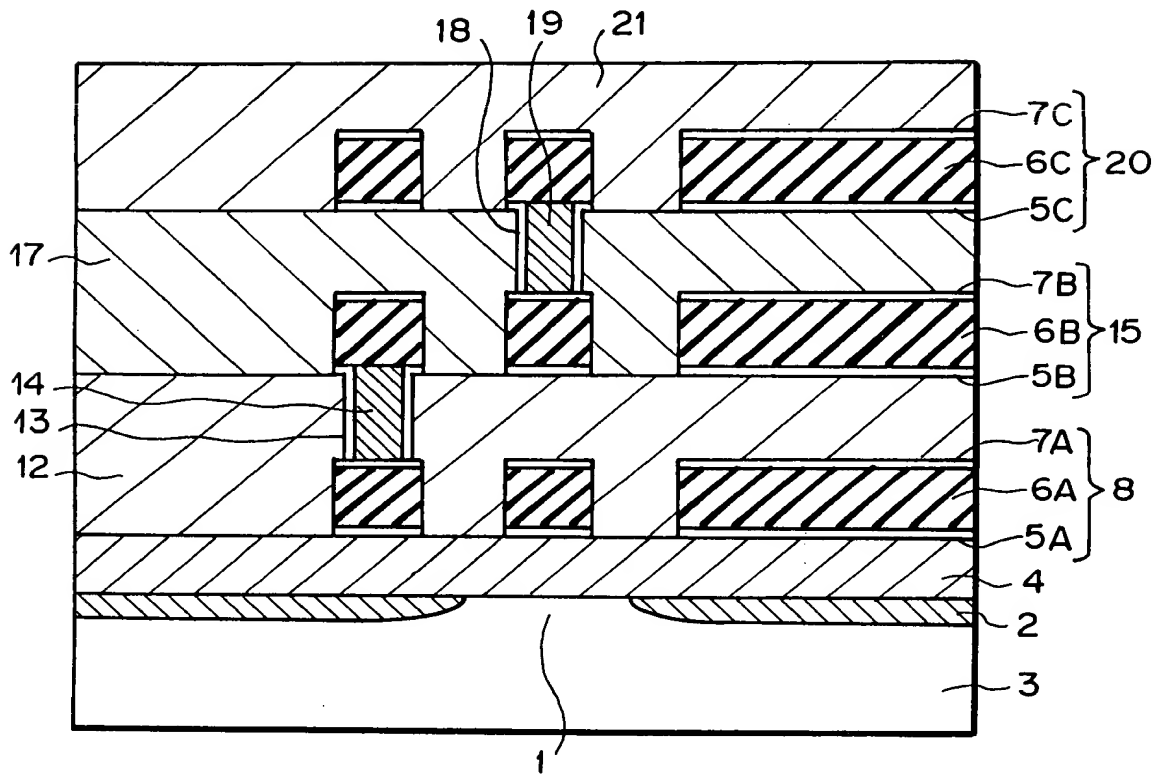


FIG. 2 (PRIOR ART)

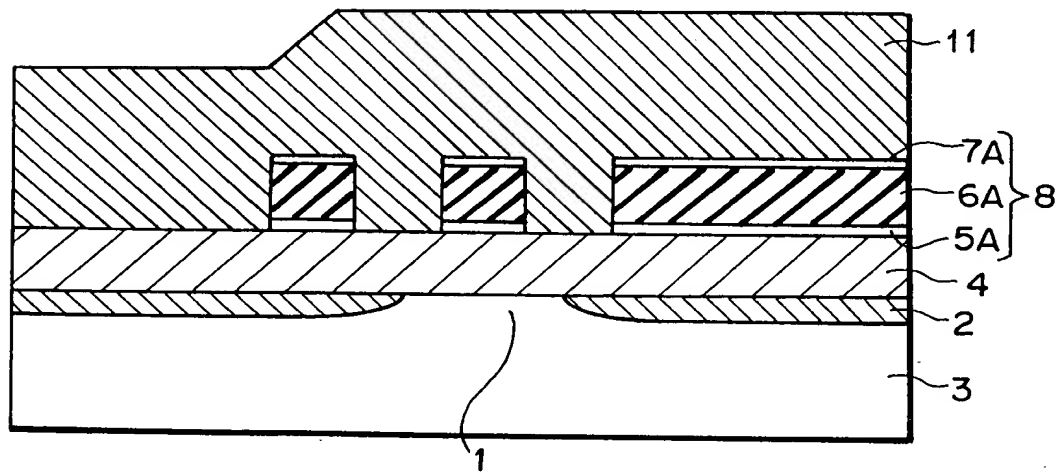


FIG. 3 (PRIOR ART)

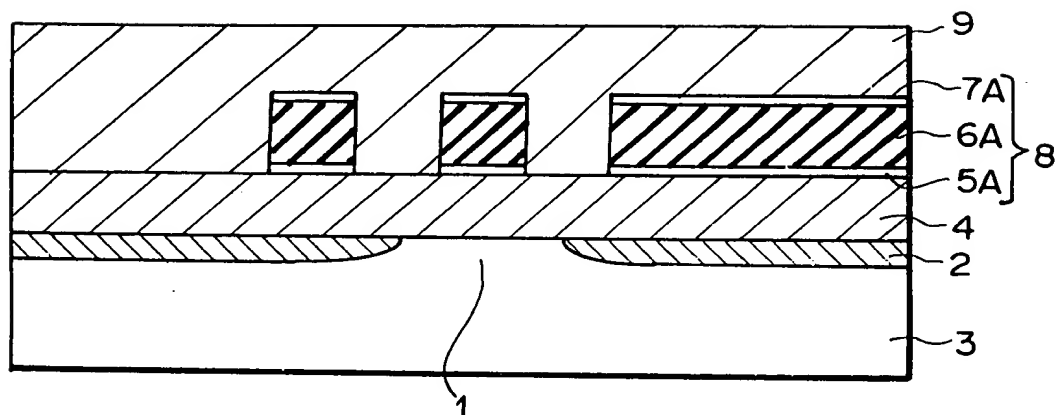


FIG. 4 (PRIOR ART)

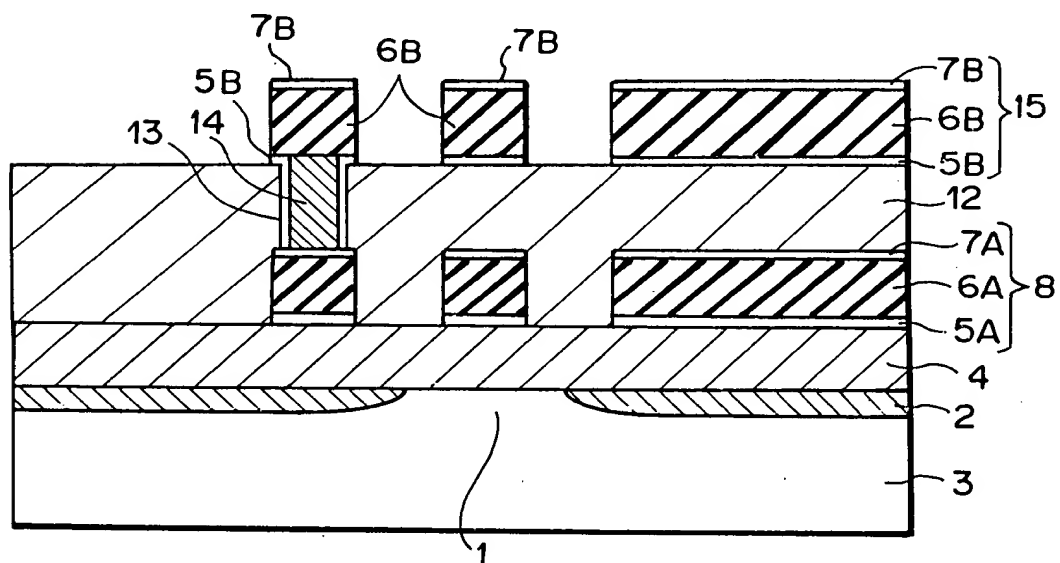


FIG. 5

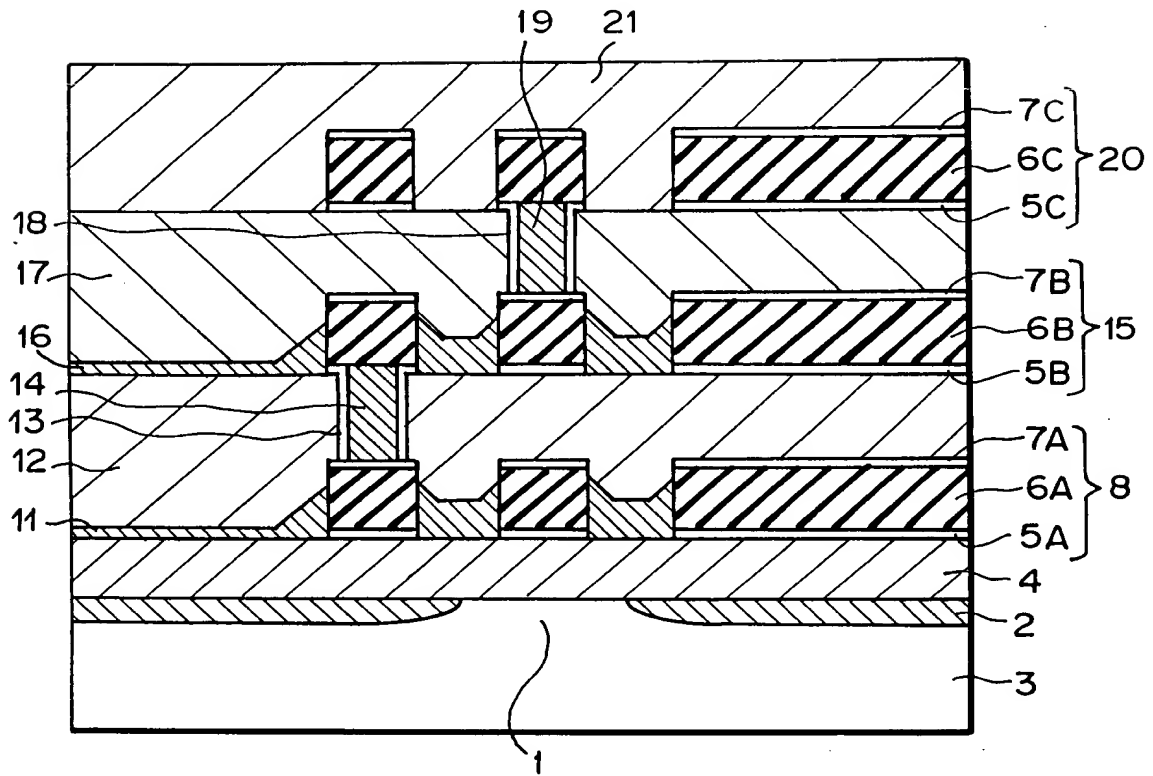


FIG. 6

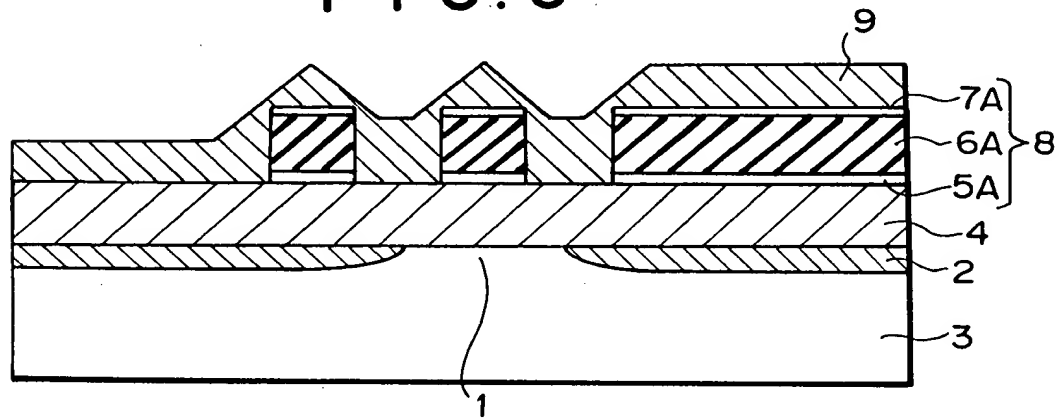


FIG. 7

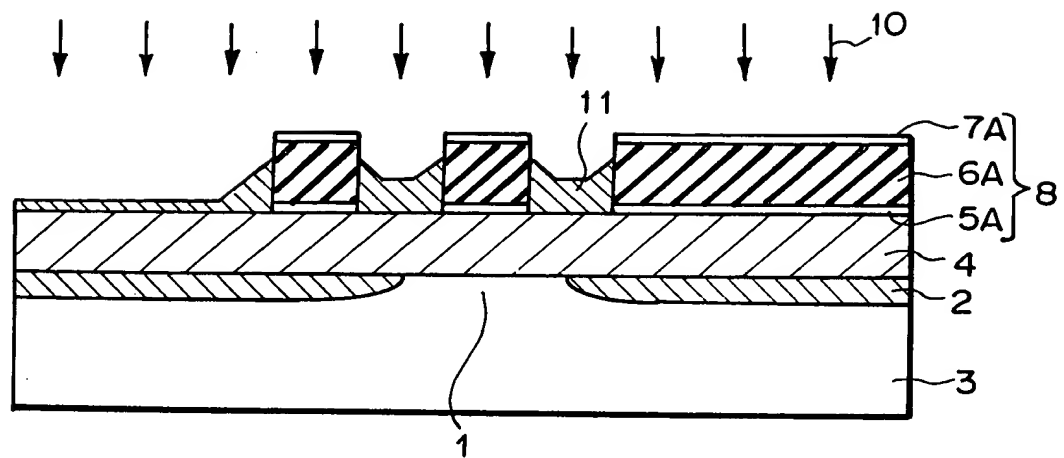


FIG. 8

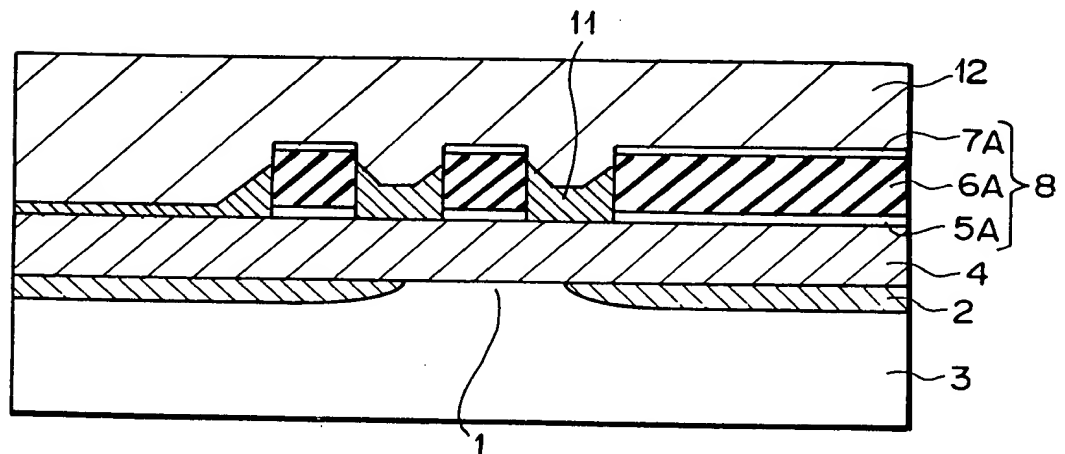


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 1 with a thin layer 2, a thick layer 4, and a patterned layer 5A. A layer 6A is formed on top of 5A, with rectangular regions 7A. A top layer 9 is also shown.

A cross-sectional view of a semiconductor device. The device consists of a substrate 1 with a recessed region 3. A thin layer 2 is formed on the surface of the substrate 1. Above layer 2 is a thick layer 4. On top of layer 4 is a layer 5A. A patterned layer 6A is formed on layer 5A, with rectangular openings. A layer 7A is formed on top of layer 6A. A final layer 9 is formed on top of layer 7A. The top surface of layer 9 is uneven, with peaks corresponding to the openings in layer 6A. Arrows 10 indicate incident light or a signal passing through the structure.

FIG. 10

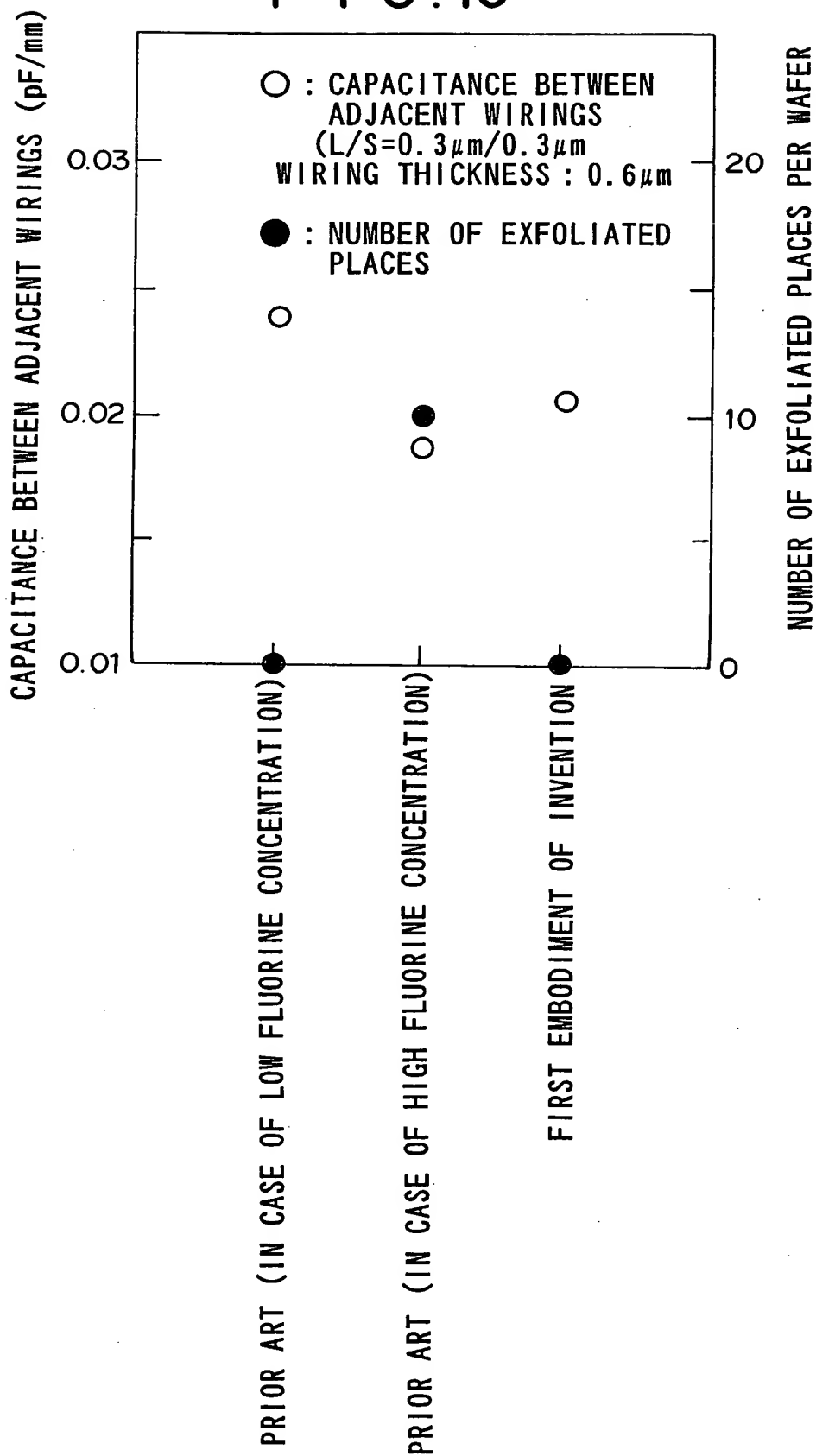


FIG. 13

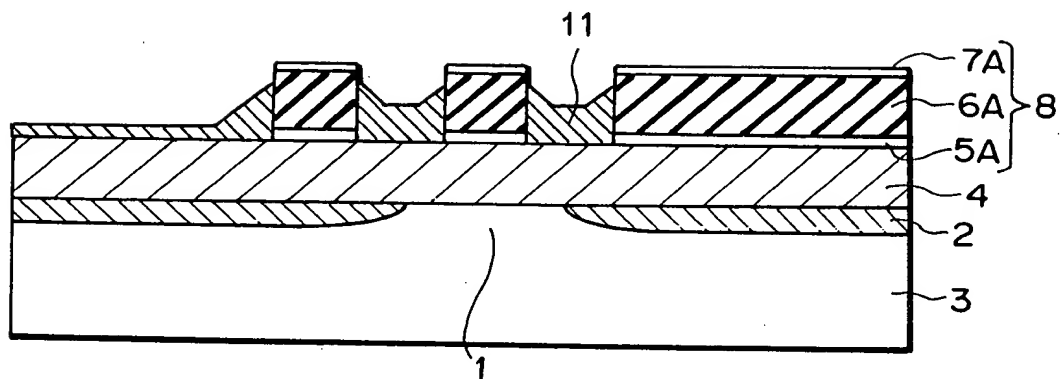


FIG. 14

